Low-temperature and Pressureless Sintering Technology for High-performance and High-temperature Interconnection of Semiconductor Devices

Guo-Quan Lu (gqlu@vt.edu)[a], Jesus N. Calata[a], Guangyin Lei[a], and Xu Chen[b]
[a]Department of Materials Science and Engineering, Virginia Tech, Blacksburg, VA, USA
[b]School of Chemical Engineering, Tianjin University, Tianjin, the People's Republic of China

Abstract

We present an interconnect technology based on low-temperature and pressureless sintering of a nanoscale metal paste to achieve high-performance and high-temperature packaging of semiconductor devices. The nanoscale metal paste, consisting of nanoparticles of silver mixed in an organic binder/solvent vehicle, can be sintered at temperatures close to 275°C. Measurements on electrical and thermal properties of the sintered die interconnect gave it at least five times better than the soldered or epoxied attachment. Die-shear tests of the sintered joints showed a bonding strength of about 25 MPa. The sintered joints exhibited excellent reliability in aging and temperature-cycling tests. Since silver melts at 961°C, the sintered interconnect can be used for wide band gap semiconductor devices (SiC or GaN), which are operable over 300°C where none of the existing solder alloys or epoxies can be used. In summary, the low-temperature sintering of nanoscale metal paste is shown to be a reliable, lead-free interconnect solution for high-temperature and high-performance packaging needs.

1. Introduction

Steady progresses made in the growth of wide bandgap semiconductor materials have led to the emergence of SiC devices for switching power electronics and GaN devices for solid-state lighting. These wide bandgap devices were shown[1-3] to have excellent properties with an added advantage of functioning at elevated temperatures in the 300°C – 500°C range. The latter opens the possibility of using these devices under extreme conditions since stringent heat sinking and cooling requirements can be relaxed. Specifically, the ability to use SiC devices at high temperatures would enable integration of power electronics circuits inside a motor, thus reducing weight and size of the motor system for automotive or aerospace applications. Moreover, the ability to support the junction temperature of a GaN LED at 350°C would allow much higher current density flowing through the device, resulting in a super bright but still reliable solid-state light source.

However, for these devices to be used under extreme conditions, high-temperature materials for interconnection and packaging have to be developed. Today, solder alloys—lead-tin and lead-free—are still the workhorse materials for interconnecting power semiconductor devices and GaN LEDs. Very few studies have addressed the need for high-performance and high-temperature interconnect solutions. Johnson *et. al.*[4] have extensively evaluated performance and reliability of several hard solders, like gold-tin, gold-germanium, and gold-silicon eutectic alloys, as high-temperature die attachment. These solders can be processed using a typical solder-reflow oven or furnace with a maximum temperature higher than the solders' melting points. Currently, these eutectic alloys are the only materials of choice for high-end applications where devices have to be operated at a junction temperature above 125°C. An example of these applications is high-power diode laser module for telecommunications systems. However, these hard solders have much lower thermal and electrical conductivities compared to those of pure noble metals, like silver.

Chuan and Lee[5] reported a high-temperature interconnect solution based on alloying of silver and indium at low temperatures. In their study, pure silver and indium thin films were separately vacuum-deposited on a device and/or substrate. Then, the joining process took place by heating the device/substrate assembly to a temperature above the melting point of indium (157°C) to allow the formation of Ag-In alloy via atomic interdiffusion. From the Ag-In binary phase diagram [6], Ag-In solid solution can be made to melt at temperatures exceeding 400°C, thus making the technique a potential candidate for high-temperature die attachment that can be processed at a lower temperature. Unfortunately, the reported low-temperature alloying process took over 20 hours to complete, a process that is too costly to be practical. Like the gold-based solder alloys, the Ag-In alloy also has poor thermal and electrical properties. Finally, the existence of several brittle intermetallic phases in the binary system poses a serious reliability threat to the long-term performance of the joints.

To take advantage of the excellent properties and high melting temperatures of noble metals for attaching devices, Scheuermann [7] and Schwarzbauer [8] explored sintering of commercial silver pastes for joining devices to a substrate. Silver, silver-palladium, and copper pastes are widely used in the fabrication of hybrid and co-fired microelectronic packages. Unfortunately, these metal pastes, consisting of micron-size metal particles in organic binder/dispersant vehicles, have to be densified at temperatures over 650°C to be useful as a conductor. To lower the sintering temperature of silver pastes below 300°C, Schwarzbauer applied a quasi-hydrostatic pressure on the device/substrate assembly to speed up the sintering kinetics of silver paste at low temperatures. It was reported that with a pressure of about 40 MPa, the silver die-attach layer underwent significant densification at 250°C and had excellent thermal and electrical properties. The sintered silver joints were also found to be highly reliable. The technique had been successfully used in the fabrication of some experimental power electronic modules at Semikron.

Recently, we reported our study [9] on the pressure-assisted sintering of commercial silver pastes for high-temperature interconnect. Our results confirm most of Schwarzbauer's findings. The sintered silver attachment had a density of 80% and thermal and electrical conductivities about half of the bulk values. However, our experience with the technique shows that the need for pressure significantly complicates the die-attach process and subjects brittle semiconductor materials to possible microscopic cracking. These are the likely reasons why manufacturers are still concerned about using the pressure-assisted sintering technique in production.

In this article, we present a low-temperature (as low as 275^{o}C), pressureless (i.e. no externally applied pressure) sintering technology that utilizes nanosilver paste to provide superior electrical, thermal and mechanical properties, and high-temperature capability for device interconnection. Some of this work has been published earlier in references [10-12]. Here, we present recent advances in the development.

2. Experimental

Details on the making of the nanoscale silver paste used in this study have been presented elsewhere[12, 13]. The material is being commercialized by NBE Technologies, LLC, 2200 Kraft Drive, Suite 1425, Blacksburg, VA 24060, USA and can be obtained by contacting nbetech@verizon.net. In this section, we describe the making of samples used for measuring the electrical conductivity of sintered silver, the bonding strength of sintered die-to-substrate joint, and the joint reliability.

2.1 Sintering time-temperature profile

Figure 1 shows an exemplary time-temperature profile used to sinter the nanosilver paste. The entire process has to be done in air to burn-out organics in the paste. The four drying steps at 50^{o}C, 75 ^{o}C, 100^{o}C, and 125^{o}C are necessary to gradually remove all the solvents in the paste prior to sintering. These incremental heating steps were accomplished with a Sikama solder reflow belt furnace. The rapid ramp-up to sintering temperatures is recommended to minimize coallesce of the nanoparticles prior to densification, which is initiated [13] by the removal of organic binder molecules in the material. We achieved rapid ramp-ups by transferring samples at 125^{o}C directly onto the hot plate set at one of the two sintering temperatures. For substrates and devices whose bonding surfaces are metallized with silver, sintering takes place at 275^{o}C for 10 mins,while 325^{o}C is needed for gold metallized surfaces to enhance interdiffusion between silver and gold.

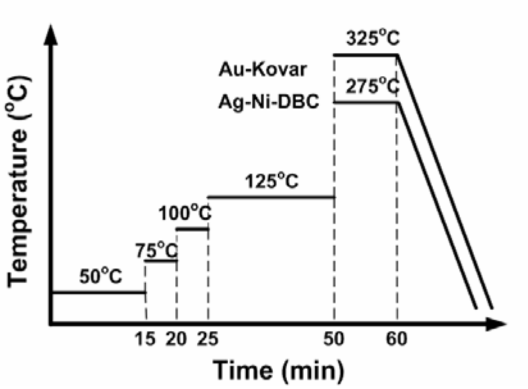
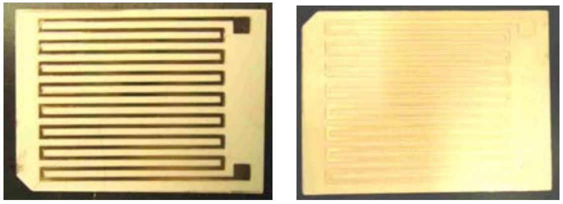


Figure 1: Recommended sintering time-temperature profile for applying the nanosilver paste to die-attach devices.

2.2 Sample Preparation

Figure 2 shows pictures of samples prepared as resistor patterns for measuring the electrical conductity of the sintered silver. The resistor pattern was formed by stencil-printing the paste on a bare alumina substrate. The print thickness was about 20 μm. After sintering, the film shrank mainly through its thickness to roughly 5~8 μm. Four-point probe test was used to get accurate measurement of the resistance. Then, from mesurements of the film thickness and width, we calculated the resistivity of the sintered silver. Finally, using the Wiedemann-Franz law [14], we estimated its thermal conductivity.

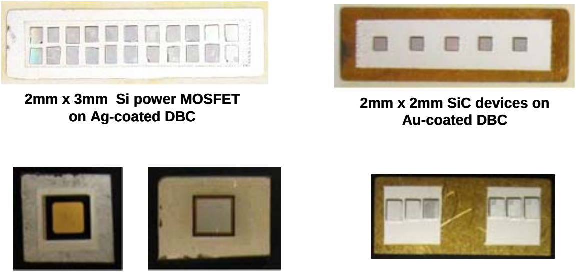


(a) **(b)**

Figure 2: (a) Stencil-printed nanosilver paste resistor pattern on a bare alumina substrate (1.7 inch x 2.3 inch); (b) after sintering with final thickness of about 40 μm.

Figure 3 shows representative pictures of devices attached on substrates. Silicon and silicon carbide devices ranging from 4 mm^{2} to 16 mm^{2} were used. Both had silver as backside metal for attchment. Four types of substrate were used: (1) alumina direct-bond-copper (DBC) electroplated with about 10 μm nickel and then 10 μm silver; (2) alumina DBC electroplated with about 10 μm nickle and then 1 μm gold; (3) Kovar metallized with a few μm-thick gold; and (4) copper electroplated with 10 μm silver. To attach the devices, we first printed the paste onto a substrate using a stencil or a spacer to a thickness between 50 μm and 100 μm, and then pressed the devices, one at a time, on the wet silver print with a little wiggling/sliding motion to ensure good wetting on device backside. Here, too much pressing pressure (>

400 kPa) should be avoided to prevent squeezing out the paste and burying or shorting the device.


2mm x 3mm Si power MOSFET on Ag-coated DBC

2mm x 2mm SiC devices on Au-coated DBC

4mm x 4mm SiC devices on Ag-coated Copper

2mm x 3mm Si MOSFET on Kovar

Figure 3: Examples of attached silicon and SiC devices on four types of substrates using the nanosilver paste and the sintering process.

As described in the previous section, devices attached on silver metallized substrates were sintered at 275^{o}C for 10 mins, while those on gold metallized substrates were sintered at 325^{o}C for 10 mins. After sintering, some attached devices were sheared off, using an in-house built tester, to determine their bonding strengths. Some of the devices attached on silver-metallized DBC were subjected to aging at 300^{o}C in an oven, then at different times were taken out and sheared off to determine the effect of aging on bonding strength. We decided on 300^{o}C for aging because it is high enough—close to 2/3 of silver melting point (ratio of the absolute temperatures)—for microstructure annealing and is low enough to avoid extensive interdiffusion between electroplated metals and underlying copper on the DBC substrate.

Finally, devices mounted on Ag-metallized DBC and Au-coated Kovar substrates were subjected to temperature cycling between -40^{o}C and 150^{o}C to evaluate the reliability of the sintered joints. The temperature cycling was carried out in a Tenney Jr. temperature cycling chamber. A soak time at the maximum and minimum temperatures of about 5 minutes each was included in the cycle. This corresponds to test condition M and soak mode 2 in the JEDEC standard temperature cycling specifications (JEDEC Standard No. 22-A104-B). The chamber is limited to less than 1 cycle per hour (condition G) such that we are unable to test for higher cycle rates.

3. Results and Discussion

Electrical resistance measurements of the sintered resistor patterns gave an average electrical conductivity of 4 x 10^{7} (Ω-m)$^{-1}$, compared to 6.3 x 10^{7} (Ω-m)$^{-1}$ for bulk silver [15]. The corresponding thermal conductivity calculated by the Wiedemann-Franz law is 290 W/m-K versus 459 W/m-K for the bulk [16]. The nearly 40% lower conductivity values found in the sintered films are attributed to a substantial porosity (about 20%) remaining in the sintered microstructure. Figure 4 is a typical scanning electron micrograph of the sintered microstructure showing a uniformly distributed micron-size pores. It is expected that denser microstructures can be achieved by going to higher sintering temperatures and longer times. But, we argue that the porous microstructure is advantageous for reliability because it lowers the elastic modulus of the sintered attachment. Attachment with lower-modulus material is more compliant to a large difference in coefficients of thermal expansion (CTEs) between the device and substrate, thus resulting in lower thermo-mechanical stresses at the joint. In our earlier work [12], we found an elastic modulus of 10 GPa for the porous material versus 67 GPa for the bulk silver.

Figure 5 shows the typical values obtained on the die-shear strengths from Ag- and Au-coated substrate surfaces. In both cases, the die-shear strengths are generally greater than 20 MPa and averaged at around 25 MPa, which is comparable to the published die-shear strengths obtained in our earlier work [11] and those found in soldered [17] and epoxied joints [18]. The larger scatter in the data is believed to come from lack of precise control over the device placement done by hand and feel. Examination of sheared-off surfaces revealed attachment silver left on the device and substrate suggesting a cohesive failure in the sintered material.

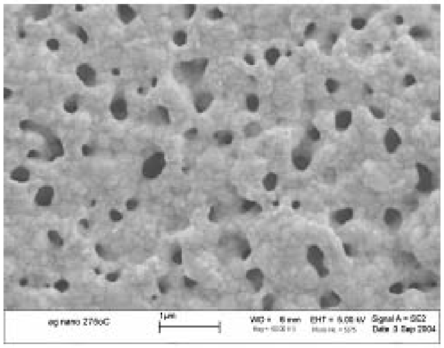


Figure 4: A typical SEM image of the sintered silver film showing a uniform distribution of about 20% micro-size posority.

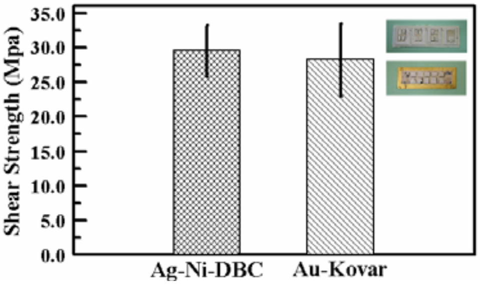


Figure 5: Measurements of die-shear strengths on devices mounted on Ag- and Au-coated substrates.

Figure 6 is a plot of die-shear strength versus aging time from devices attached on Ag-coated DBC substrates that were heated at 300^{o}C in an oven. Taking into consideration the scatter in die-shear strengths, we believe that the aging had no significant effect on the joint strength. In a recent study on using lead-free solder for die-attach [19], the authors reported a drastic decrease in bonding strength after aging. The decrease was attributed to microstructural changes in the solder alloy at the aging temperature of 150°C. In our case, since the aging temperature of 300°C is much lower than the 961°C melting point of silver and the sintering process had spent much of the surface/interfacial free energies, we do not expect the once sintered microstructure to undergo significant microstructural evolution. The sintered microstruture is likely to densify a little further at the aging temperature. This, we believe, will strengthen the joint by increasing the cohesion of the attachment as well as adhesion between the attachment and its adherents (i.e. device and substrate).

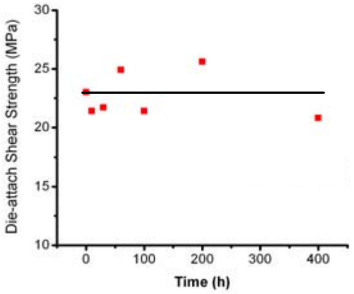


Figure 6: Measurements of die-shear strengths on devices mounted on Ag- and Au-coated substrates.

Figure 7 (a) and (b) are plots of die-shear strength vs. number of cycles from the temperature-cyling tests on devices attached to Au-coated Kovar and silver-coated DBC substrates, respectively. In both, the die-shear strength decreased slowly with number of cycles, but still retained about 20 MPa after 600 cycles. The cycling experiment was stopped because we ran out of samples to test. New batches of samples have been made to allow us to extend the temperature-cycling experiemnt.

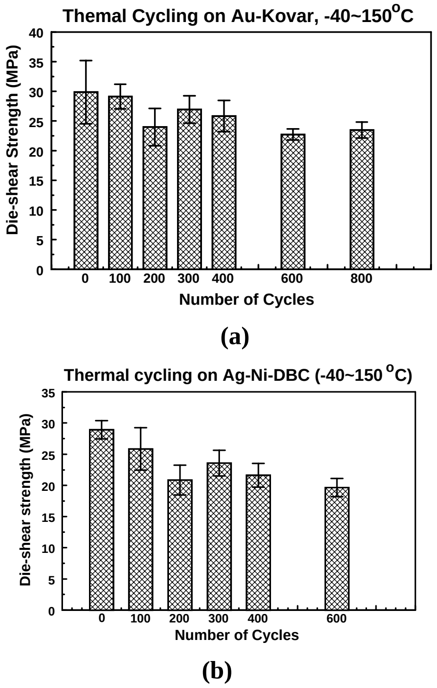


Figure 7: Plots of die-shear strength versus number of cycles from -40°C-150°C temperature-cycling tests of (a) devices mounted on Au-coated Kovar substrate and (b) Ag-coated DBC.

To demonstrate that the low-temperature sintering technique can be used for die-attach as well as for interconnecting other terminals, we made packages of IGBT devices shown in figure 8. First, the devices were attached on Ag-coated DBC by the sintering process at 275°C, and then copper straps that were electroplated with μm-thick silver were interconnected to the other terminals by the second sintering process. In the package shown on the left, the gate terminal was wire-bonded; while on the right the gate interconnection was formed by sintering along with the source interconnection. A benefit of using the sintering technique is that once the material is sintered it will not melt unless it is heated to 961°C (the melting point of silver). Thus, the same sintering process can be repeatedly used in a packaging process that involves multiple joining steps. This eliminates the need to design a hierarchy of process temperatures necessary to accommodate different reflow schedules when solder alloys are used.

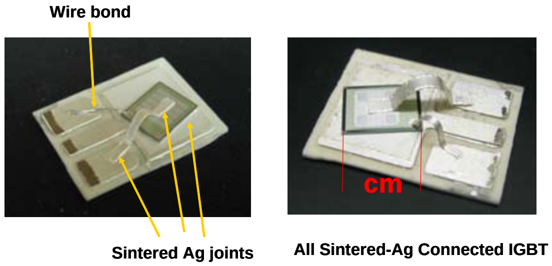


Figure 8: Examples of IGBT devices interconnected on both attached on using the low-temperature sintering process.

4. Conclusions

Table 1 summarizes the characteristics of widely used die-attach materials together with those obtained in this study on the low-temperature and pressureless sintered nanoscale silver paste. Since the sintered joints are made of pure silver, they have substantially higher (at least five times) electrical and thermal conductivities than those of the other materials. The relative properties are expected to be even better for the sintered silver joints when devices are powered up since the other materials would be operating much closer to their melting/decomposition temperatures.

Because of its relative density of roughly 80%, the sintered silver has a low elastic modulus of about 10 GPa, which lowers thermo-mechanical stresses at the joints, thus improves joint reliability. Results of our temperature-cycling tests showed high reliability of the sintered joints. As large voids are known to form in a soldered die-attach layer, in the sintered attachment residual pores are small (micron-size) and uniformly distributed, thus eliminating hot spots underneath the device. Furthermore, formation of brittle intermetallic phases at soldered joints is always a concern for joint reliability. This, however, is not a concern with the sintered joint since elemental metal is used.

Table 1: Summary of typical properties of commerical die-attach materials and nanosilver paste of this work.

	Processing temperature	Max. use temperature	Electrical conductivity 10^7 (O-m)$^{-1}$	Thermal conductivity (W/K-m)	Die-shear Strength (MPa)
Lead-tin solder	217°C	< 183°C	0.69	51	35
Lead-free solder	260°C	< 225°C	0.75	70	35
Gold-tin solder	310°C	< 280°C	0.625	58	30 - 60
Silver epoxy	100 – 200°C	< 200°C	0.1	10	10 - 40
P-less Sintered nano-Ag	~ 275°C	< 961°C*	4.0	290	20 – 35

As the low-temperature sintering technology for interconnecting devices does not require external pressure, and the nanosilver paste can be readily printed or dispensed, the nanosilver paste can be a one-to-one replacement for solders and epoxies that are commonly used in today's manufacturing processes. Finally, by properly selecting diffusion-barrier and encapsulation materials to prevent silver electromigration, the sintering technology with the nanosilver paste can be a viable interconnection solution for high-temperature packages.

Acknowledgments

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References

1. Wang, X.W., W. J. Zhu, X. Guo, T. P. Ma, J. B. Tucker, and M.V. Rao, *High temperature (450°C) reliable NMISFET's on p-type 6H-SiC*. IEEE IEDM Technical Digest, 1999: p. 209 - 212.
2. Wondrak, W., R. Held, E. Niemann, and U. Schmid, *SiC devices for advanced power and high-temperature applications*. IEEE Transactions on Industrial Electronics, 2001. **48**(2): p. 307-308.
3. Singh, R., S. H. Ryu, D. C. Capell, and J. W. Palmour, *High temperature SiC trench gate p-IGBTs*. IEEE Transactions on Electron Devices, 2003. **50**: p. 774 - 784.
4. Johnson, R.W., M. Palmer, C. Wang, and Y. Liu, *Packaging Materials and Approaches for High Temperature SiC Power Devices*. Advancing Microelectronics, 2004. **31**(1): p. 8-11.
5. Chuang, R.W., and C. C. Lee, *Silver-Indium Joints Produced at Low Temperature for High Temperature Devices*. IEEE Transactions on Components and Packaging Technologies, 2002. **25**(3): p. 453-458.
6. Massalski, T.B., ed. *Binary Alloy Phase Diagrams*. 2nd Edition ed. 1990, ASM International: Materials Park, OH. 34.
7. Scheuermann, U., *Low Temperature Joining Technology - A High Reliability Alternative to Solder Contacts*, in *Workshop on Metal Ceramic Composites for Functional Application*. 1997: Vienna.
8. Schwarzhauer, H., *Method of Securing Electronic Components to a Substrate*. 1998: US.
9. Zhang, Z., and G-Q. Lu, *Pressure-Assisted Low-Temperature Sintering of Silver Paste as an Alternative Die-Attach Solution to Solder Reflow*. IEEE Transactions on Electronics Packaging Manufacturing, 2002. **25**(4): p. 279 - 283.
10. Zhang, Z., J. N. Calata, J. G. Bai, and G-Q. Lu. *Nanoscale Silver Sintering for High-Temperature Packaging of Semiconductor Devices*. in *Proc. of 2004 TMS Annual Meeting & Exhibition*. 2004. Charlotte, NC.
11. Bai, J.G., and G-Q. Lu, *Thermomechanical Reliability of Low-Temperature Sintered Silver Die-Attached SiC Power Device Assembly*. IEEE Trans. on Device and Materials Reliability, 2006. **6**(3): p. 436 - 441.
12. Bai, J.G., Z. Z. Zhang, J. N. Calata, and G-Q. Lu, *Low-Temperature Sintered Nanoscale Silver as a Novel Semiconductor Device-Metallized Substrate Interconnect Material*. IEEE Transactions on Components and Packaging Technologies 2006. **29**(3): p. 589 - 593.
13. Bai, J.G., *Ph.D. Dissertation: Low-Temperature Sintering of Nanoscale Silver Paste for Semiconductor Device Interconnection*, in *Materials Science and Engineering*. 2005, Virginia Polytechnic Institute and State University: Blacksburg.
14. Ashcroft, N.W., and N.D. Mermin, *Solid State Physics*. 1976: Holt, Rinehart, and Winston.
15. Matula, R.A., J. Phys. Chem. Ref. Data, 1979. **8**(4): p. 1147.
16. Ho, C.Y., R.W. Powell, and P.E. Liley, J. Phys. Chem. Ref. Data, 1972. **1**: p. 279.
17. Hwang, J.S., ed. *Chapter Six: Solder technologies for electronic packaging and assembly*. 3rd Edition ed. Electronic Packaging and Interconnection Handbook, ed. C.A. Harper. 2000, McGraw-Hill: New York.
18. Nguyen, G.P., et al.,, *Conductive adhesives*. Circuits Assembly, 1993: p. 36.
19. Anderson, I.E., and J.L. Harringa, *Elevated temperature aging of solder joints based on Sn-Ag-Cu-Effects on joint microstructure and shear strength*. J. Electron. Mater. , 2004. **33**: p. 1485.